WHAT IS CLAIMED IS:

1. An electronic memory device tester, comprising:

an input, arranged to receive seed data which has a first number, p, of seed data bits, from a computer; and

a data generator arranged to generate an array of prepared data having a second number, q, of prepared data bits, where q>p, and arranged to generate from the prepared data a test data pattern for writing to an electronic memory device to be tested.

2. The tester of claim 1, in which the data generator comprises:

a plurality of data write registers arranged to receive the seed data from the computer and to generate therefrom the said prepared data; and

a test pattern generator arranged to generator one of a plurality of test data patterns from the prepared data.

3. The tester of claim 2, in which each data write register comprises an 8 bit data latch to which an 8 bit seed data word may be individually written.

4. The tester of claim 3, in which each of the 8 bit data latches is arranged to receive the same 8 bit seed data word.

5. The tester of claim 3, in which at least some of the 8 bit data latches are arranged to receive

different 8 bit seed data words.

6. The memory tester of claim 1, in which the input is further arranged to receive a clock signal from the computer and to control the writing of the test data pattern to the memory device on the basis of that clock signal.

7. The tester of claim 1, further comprising:

a data reader arranged to read the test data pattern that has been written to the electronic memory device, and a data comparator to compare it with the test data pattern generated by the data generator, and to provide an output indicative of errors in the memory device being tested.

8. The memory tester of claim 7, in which the output of the data comparator is an error signal, and wherein, in response to the error signal being generated, the data reader is arranged to stop reading test data written to the memory device.

9. The memory tester of claim 7, further comprising a multiplexer arranged to receive failure data representative of errors in the memory device to be tested, and to output multiplexed failure data.

10. The memory tester of claim 1, further comprising an address generator arranged to generate a memory address representative of an address in the memory device to be tested, and to which test data from the test data pattern is to be written.

11. The memory tester of claim 10, further comprising a plurality of upper address registers arranged to receive upper address data from a computer and to generate a latched upper address signal therefrom.

12. The memory tester of claim 11, in which the address generator receives, as a first input, the said latched upper address signal, and receives as a second input, a lower address signal from the computer, the memory address being generated in dependence upon the upper and lower address signals under the control of a clock signal.

13. The memory tester of claim 12, in which the address generator generates an address command identifying a linear memory address as the combination of a row address and a column address.

14. The memory tester of claim 13, further comprising an addressing mode selector arranged to adjust the address command so that linear memory addresses of different widths may be addressed, and/or to adjust the address command so as to switch the addressing mode between symmetric and asymmetric.

15. The memory tester of claim 1, further comprising a memory heater arranged to heat the memory device when in use.

16. The memory tester of claim 15, in which the

memory heater comprises a heat cycle latch arranged to increase the cycle rate of a write cycle signal for output to the memory device, so as to cause an increase in the heat dissipated by the memory device when in use.

17. Apparatus comprising:

a computer system comprising a central processing unit in communication with a computer system bus, and means for controlling access to the computer system bus;

an electronic memory device in communication with a memory device bus, the memory device having a plurality of readable and writable memory elements; and

an electronic memory device tester comprising:

an input, arranged to receive seed data which has a first number, p, of seed data bits, from a computer; and

a data generator arranged to generate an array of prepared data having a second number, q, of prepared data bits, where q>p, and arranged to generate from the prepared data a test data pattern for writing to an electronic memory device to be tested;

wherein the computer system is arranged to generate the seed data, the memory tester is arranged to receive the seed data at its input via the computer system bus, and the memory device is arranged to receive the test pattern data from the memory tester via the memory device bus.

18. The apparatus of claim 17, in which the computer system bus has a first bus width and the

memory device bus has a second bus width larger than the first bus width.

19. A method of writing data to an electronic memory device to be tested, comprising the steps of:

(a) generating, in a separate computer, seed data having a first number, p, of seed data bits;

(b) receiving, in a memory tester, the seed data;

(c) generating, from the received seed data, an array of prepared data having a second number, q, of prepared data bits, where q>p;

(d) generating, from the prepared data, a test data pattern; and

(e) writing the test data pattern to the electronic memory device to be tested.

20. The method of claim 19, in which the step (c) of generating the array of prepared data further comprises:

writing the received seed data to each of a plurality of data latches.

21. The method of claim 20, further comprising writing the same received seed data to each of the plurality of data latches.

22. The method of claim 20, further comprising writing a first array of received seed data to a first data latch, and writing at least one further array of different received seed data to at least one further

data latch.

23. The method of claim 19, further comprising:

receiving in the memory tester, a clock signal from the computer; and

controlling the writing of the test data pattern to the memory device on the basis of that clock signal.

24. A method of testing an electronic memory device, comprising:

writing test data to the memory device, the writing of test data comprising the steps of:

(a) generating, in a separate computer, seed data having a first number, p, of seed data bits;

(b) receiving, in a memory tester, the seed data;

(c) generating, from the received seed data, an array of prepared data having a second number, q, of prepared data bits, where q>p;

(d) generating, from the prepared data, a test data pattern; and

(e) writing the test data pattern to the electronic memory device to be tested.

reading the test data pattern previously written to the memory device;

comparing the read test data pattern with the test data pattern that was written to the memory device; and

generating an output indicative of errors in the memory device under test, when the said read test data pattern does not match the said written test data pattern.

25. The method of claim 24, in which the generated output is an error signal, the method further comprising:

the step of reading the test pattern data in response to the generated error signal.

26. The method of claim 19, further comprising:

receiving, in the memory tester, upper address data from the computer;

generating a latched upper address signal therefrom;

receiving, in the memory tester, a lower address signal from the computer; and

addressing the memory device to be written to in dependence upon the upper and lower address signals, under the control of a clock signal.

27. The method of claim 26, further comprising:

generating an address command identifying a linear memory address by a combination of a row address and a column address within the memory device.

28. The method of claim 27, further comprising:

adjusting the address command to permit linear memory addresses of different address widths to be addressed.

29. The method of claim 27, further comprising:

adjusting the address command to permit either symmetric or asymmetric linear memory addresses to be addressed.

30. The method of claim 19, in which the memory device to be tested is Dynamic Random Access Memory (DRAM), the method further comprising:

refreshing the DRAM on a periodic basis under the control of the external computer.

31. An electronic memory device tester, comprising:

input means for receiving seed data which has a first number, p, of seed data bits, from processing means; and

data generator means for generating an array of prepared data having a second number, q, of prepared data bits, where $q>p$, and arranged to generate from the prepared data a test data pattern for writing to an electronic memory device to be tested.